Mod5272 Hardware Design Notes

Application Note

Revision 1.1
January 27, 2004
Document Status: Release

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Introduction

This document provides hardware design information, tips and guidelines for using the Mod5272 with external hardware.

Interrupt Signals

Four interrupt signals are available on connector J2: *IRQ1, *IRQ3, *IRQ5, *IRQ6/PA15. These signals are all pulled to 3.3V through a 4.7K resistor.

QSPI

The QSPI signals are configured as show in the table below. Note that the QSPI CS0 signal is pulled to ground as required to enable the data bus at power-up, which is needed by the Flash and SDRAM on the module. Thus, QSPI CS0 cannot be used as a QSPI chip select.

Signal	Description
SPI_CLK	Pulled to 3.3V with 4.7K ohms
SPI_DIN	Floating
SPI_DOUT	Pulled to 3.3V with 4.7K ohms
*SPI_CS0	Pulled to GND with 4.7K ohms
*SPI_CS1	Floating
*SPI_CS2	Floating
*SPI_CS3	Floating

TIP Signal and External Data Bus Connections

The TIP signal is the logical AND of *CS1, *CS2 and *CS3. TIP can used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 - D31

Timers and UART0 External Baud Rate Clock

TIN0 and PB4/UART0 are shorted together, and this signal is brought out on J2 pin 31. Due to the limited board space for connectors, this allows you to choose either an external baud rate clock input, or a timer input.

TIN1 is floating.

USB

The ColdFire 5272 processor supports USB device mode only. A 48MHz oscillator must be installed in location U8 of the Mod5272. This oscillator can be purchased from Digikey, part number:
ECS-3953M-480-ND

Chip Selects

The chip selects CS1, CS2 and CS3 are floating outputs.

Reset Signals

Signal	Description	Implementation
*RSTI	Reset Input	Pulled to 3.3V through 4.7K ohms on the module
*RST0	Reset Output	Output from processor

Bus Control Signals

Signal	Description	Implementation
R/*W	Read/Write	Floating
*OE	Output Enable	Floating
*BS2, *BS3	Byte strobes	Floating
*TIP	Transfer in Progress	Logical AND of chip selects *CS1, *CS2 and *CS3
*TA	Transfer Ack	Floating

System Clock Signal

The system clock pin provides an output of 62.5 MHz.

UARTS

The NNDK Module Development Board has 330 ohm resistors in series with the UART RX lines. This was done to make the development board compatible with the ColdFire 5282, which has a maximum current specification of 25mA if the input voltage is above 3.3VDC. The resistors are not required for the ColdFire 5272. The resistors are present on board revisions 1.1 and later.