Mod5272 GPIO Configuration

Application Note

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Introduction

The Mod5272 provides up to 24 pins of General Purpose I/O. Each pin on the MCF5272 processor can have up to four functions. The function of each pin is determined by setting in configuration and control registers (except for Port C, which is configured by the WSEL pin logic level during device reset). This application note will provide explanations and programming examples on how to configure them as GPIO.

Port A

Port A is one of the three GPIO ports on the MCF5272 and provides up to 16 GPIO signals. For more information on Port A, please refer to chapter 17 of the Motorola 5272 User Manual.

Port A Data Direction Register (PADDR): The PADDR determines the signal direction of each parallel port pin programmed as a GPIO port in the PACNT. (Figure 17-4 in the Motorola 5272 User Manual.). Setting a bit field to 0 configures the pin as an input, setting it to 1 configures the pin as an output.

15	0
Field	PADDR
Reset	0000_0000_0000_0000
R/W	Read/Write

Port A Data Register (PADAT): The PADAT value for inputs corresponds to the logic level at the pin; for outputs, the value corresponds to the logic level driven onto the pin. Note: PADAT has no effect on pins that have not been configured for GPIO. (Figure 17-7 in the Motorola 5272 User Manual.)

15	0
Field	PADAT
Reset	Undefined
R/W	Read/Write

Port A GPIO Pins: PACNT is used to configure the pins assigned to signals that are multiplexed with GPIO port A. (For additional information see tables 17-3 and 17-4 in the Motorola 5272 User Manual.)

Mod5272 Con/Pin #	Bits	Signal Name	Description	Drive Capability
J2 - 33	11-10	PA5 (PACNT5)	Configure pin E2 00 PA5 01 USB_TxEN 1x Reserved	2 mA
J2 - 39	1-0	PA0 (PACNT0)	Configure pin D2 00 PA0 01 USB_TP 1x Reserved	2 mA
J2 - 42	3-2	PA1 (PACNT1)	Configure pin D1 00 PA1 01 USB_RP 1x Reserved	2 mA
J2 - 48	31-30	PA15/IRQ 6 (PACNT15)	Configure pin M3. If this pin is programmed to function as INT6, it is not available as a GPIO. 00 PA15 01 DGNT1 1x Reserved	2 mA

Port A Example Code

Example 1: Configure pins 33, 39, 42 and 48 as outputs

```
#include <..\mod5272\system\sim5272.h>

sim.paddr = 0xFFFF; // Configure DDR so all pins are outputs
sim.padat = 0x0020; // Set pin 33 high
sim.padat = 0x0001; // Set pin 39 high
sim.padat = 0x0002; // Set pin 42 high
sim.padat = 0x8000; // Set pin 48 high

sim.padat = 0x0;    // Set all pins low
```

Example 2: Configure pins as inputs

```
#include <..\mod5272\system\sim5272.h>

sim.paddr = 0x0;           // Configure DDR so all pins are inputs
WORD value_of_pins = sim.padat; // Read pin values as inputs
```

Port B

Port B is one of the three GPIO ports on the MCF5272 and provides up to 16 GPIO signals. For more information on Port B, please refer to chapter 17 of the Motorola 5272 User Manual.

Port B Data Direction Register (PBDDR): The PBDDR determines the signal direction of each parallel port pin programmed as a GPIO port in the PBCNT. (Figure 17-5 in the Motorola 5272 User Manual.). Setting a bit field to 0 configures the pin as an input, setting it to 1 configures the pin as an output.

15	0
Field	PBDDR
Reset	0000_0000_0000_0000
R/W	Read/Write

Port B Data Register (PBDAT): The PBDAT value for inputs corresponds to the logic level at the pin; for outputs, the value corresponds to the logic level driven onto the pin. Note: PBDAT has no effect on pins that have not been configured for GPIO. (Figure 17-7 in the Motorola 5272 User Manual.)

15	0
Field	PBDAT
Reset	Undefined
R/W	Read/Write

Port B GPIO Pins: PBCNT is used to configure the pins assigned to signals that are multiplexed with GPIO port B. (For additional information see tables 17-5 and 17-6 in the Motorola 5272 User Manual.)

Mod5272 Con/Pin #	**Bits**	**Signal Name**	**Description**	**Drive Capability**
J2-3	0-1	PB0 URTO_TX	Configure Pin H4 00 PB0 01 URT0_TX 1x Reserved	4mA
J2-4	2-3	PB1 URT0_RX TIN3*	Configure Pin H1 00 PB1 01 URT0_RX/TIN3 1x Reserved	2mA
J2 - 29	5-4	PB2 (H2) PBCNT2	Configure Pin H2 00 PB2 01 URT0_CTS 1x Reserved	2 mA
J2 - 38	7-6	PB3 (H3) PBCNT3	Configure Pin H3 00 PB3 01 URT0_RTS 1x Reserved	4 mA

*The signal URT0_RX is always internally connected to TIN3 inside the 5272 processor

Port B Example Code

Example 1: Configure pins 29 and 38 as outputs

```
#include <..\mod5272\system\sim5272.h>

sim.pbddr = 0xFFFF; // Configure DDR so all pins are outputs
sim.pbdat = 0x0004; // Set pin 29 high
sim.pbdat = 0x0008; // Set pin 38 high
sim.pbdat = 0x0;    // Set both pins low
```

Example 2: Configure pins as inputs

```
#include <..\mod5272\system\sim5272.h>

sim.pbddr = 0x0;           // Configure DDR so all pins are inputs
WORD value_of_pins = sim.pbdat; // Read pin values as inputs
```

Port C

Port C is one of the three GPIO ports on the MCF5272 and provides up to 16 GPIO signals. There is not a configuration register for Port C; because its pins are configured by WSEL during device reset. For more information on Port C, please refer to chapter 17 of the Motorola 5272 User Manual.

Mod5272 Port C Pinouts

Mod5272 Con/Pin #	Signal Name	Drive Capability
J2 - 6	PC14	6 mA
J2 - 7	PC13	6 mA
J2 - 8	PC15	6 mA
J2 - 9	PC11	6 mA
J2 - 10	PC12	6 mA
J2 - 11	PC10	6 mA
J2 - 12	PC9	6 mA
J2 - 13	PC8	6 mA
J2 - 15	PC0	6 mA
J2 - 16	PC1	6 mA
J2 - 17	PC4	6 mA
J2 - 18	PC2	6 mA
J2 - 19	PC5	6 mA
J2 - 20	PC6	6 mA
J2 - 23	PC3	6 mA
J2 - 24	PC7	6 mA

Port C Data Direction Register (PCDDR): The PCDDR determines the signal direction of each parallel port pin programmed as a GPIO port in the PCCNT. (Figure 17-6 in the Motorola 5272 User Manual.). Setting a bit field to 0 configures the pin as an input, setting it to 1 configures the pin as an output.

15	0
Field	PCDDR
Reset	0000_0000_0000_0000
R/W	Read/Write

Port C Data Register (PCDAT): The PCDAT value for inputs corresponds to the logic level at the pin; for outputs, the value corresponds to the logic level driven onto the pin. Note: PCDAT has no effect on pins that have not been configured for GPIO. (Figure 17-7 in the Motorola 5272 User Manual.)

15	0
Field	PCDAT
Reset	Undefined
R/W	Read/Write

Using Port C With Revision 1.01 Assemblies

A jumper must be installed for revision 1.01of the Mod5272 boards to control the WSEL pin during reset. This problem has been corrected in board revisions higher than 1.01. If you are not using the SPI port, there is a simple work around: Tie the SPI DOUT/WSEL signal on pin J2-28 to 3.3V. It is ok to tie the J2-28 pin to 3V permanently.

Port C Example Code

Example 1: Configure pins as outputs

```
#include <..\mod5272\system\sim5272.h>

sim.pcddr = 0xFFFF; // Configure DDR so all pins are outputs
sim.pcdat = 0xFFFF; // Set all pins high
sim.pcdat = 0x0;    // Set all pins low

sim.pcdat |= 0x8000;       // Set pc15 high
sim.pcdat &= ~(0x8000);    // Set pc15 low
```

Example 2: Configure pins as inputs

```
#include <..\mod5272\system\sim5272.h>

sim.pcddr = 0x0;           // Configure DDR so all pins are inputs
WORD value_pc = sim.pcdat; // Read pin values
```