Mod5270 Hardware Design Notes

Application Note

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1 Introduction

This document provides hardware design information, tips and guidelines for using the Mod5270 with external hardware. This document uses the following terminology:

Output: indicates an output from the microprocessor. In general, the instantaneous maximum current for a single pin is 25 mA. The sustained current drive is 5 mA. Please see the document, "MCF5271 Integrated Microprocessor Hardware Specification" for more information.

Input: indicates an input to the Mod5270.

Asserted: The asserted state of a signal depends upon the signal description. If a signal is active low as defined by the '*' character preceding the signal name, then the asserted state is low. If a signal is active high, then the asserted state is high.

Negated: The negated state of a signal depends upon the signal description. If a signal is active low as defined by the '*' character preceding the signal name, then the negated state is high. If a signal is active high, then the negated state is low.

Other important reference materials that should be consulted before completing a hardware design are:

- Freescale Mod5270/71 Reference Manual
- Freescale Mod5270/71 Integrated Microprocessor Hardware Specification

Both of these documents were installed with your NetBurner Development Kit installation.

2 Interrupt Signals

Four interrupt signals are available on connector J2: *IRQ1, *IRQ3, *IRQ5 and *IRQ7. These signals are active low inputs with 3.3V pull-ups through individual 4.7K resistors on the Mod5270.

3 QSPI

The QSPI signals are configured as show in the table below.

Signal	**Description**
SPI_CLK	Output. Serial clock
SPI_DIN	Floating Input. Serial data input
SPI_DOUT	Output. Serial data output.
*SPI_CS0	Output. Peripheral chip select.
*SPI_CS1	Output. Peripheral chip select.
*SPI_CS2	Not available on the Mod5270
*SPI_CS3	Output. Peripheral chip select.

4 I2C

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications that require occasional communication between many devices over a short distance. For I2C compliance, all devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors. **You will need to add the external pull-up resistors to your design**. Refer to the I2C section of the Freescale MCF5270/71 Reference manual for details on configuration, loading and speed.

The I2C signals on the Mod5270 can be configured to come out on JP2 pins 39 and 42 by default. If you wish to use these pins as GPIO, the I2C signals can be configured to use JP2 pins 25 and 27, as an alternate function to QSPI DIN and CLK.

Signal	Description
I2C_SCL	Open collector, Serial clock
I2C_SDA	Open collector, Data input/output

5 Reset Signals

Signal	**Description**	**Implementation**
*RSTI	Reset Input	Input with 4.7k pull-up to 3.3V. Asserted to enter reset exception processing.
*RST0	Reset Output	Output from processor. Automatically asserted with *RSTI. Negation indicates that the PLL has regained it’s lock.

6 Using the External Address and Data Bus

The Mod5270 provides an external address and data bus that can be used to interface to external hardware. A typical interface involves a chip select to enable the external hardware, and the address/data bus to read/write data. More advanced interfaces may use one or more of the Bus Control Signals to enable outputs and acknowledge data transfers. The bus speed is one half the processor clock speed of 147.456 MHz. This section provides an overview of the signals, please refer to the Freescale MCF5270/71 Reference Manual for additional information.

6.1 Chip Selects

The chip selects *CS1, *CS2 and *CS3 are active low output signals. Each chip select can be independently programmed for an address location, as well as for masking, port size, read/write, wait-state generation, and internal/external termination.

Each chip select has a dedicated set of registers for configuration and control. Chip select address registers (CSARn) control the base address of the chip select, chip select mask registers (CSMRn) provide 16-bit address masking and access control, and chip select control registers (CSCRn) provide port size and burst capability indication, wait-state generation, and automatic acknowledge generation features. See the Freescale MCF5270/71 Reference Manual, Chip Select Module section for more details.

6.2 Address and Data Bus Signals

The Mod5270 provides 16 address lines, A[0-15], which provide 64k addressable locations. Used in conjunction with the chip selects, you can have up to three 64k byte address spaces, or combine them into a seamless 3 x 64k address space by using all three chip selects for a single device.

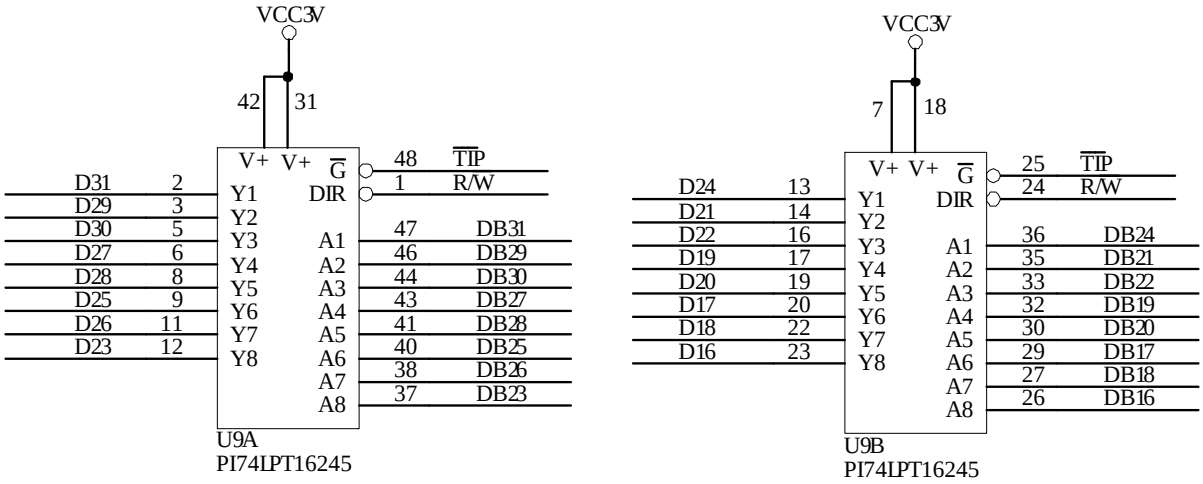
The Mod5270 provides an external 16-bit data bus, D[16-31]. Notice that the signal names start at D16, not D0. Freescale processors use the upper data bus signals. A 16-bit interface will use D16-D31, where D16 is the least significant bit. An 8-bit interface will use D25-D31, where D25 is the least significant bit.

6.3 Bus Control Signals

Signal	Description	Implementation
R/*W	Read/Write	Output. Indicates the direction of the data transfer on the bus.
*OE	Output Enable	Output. Indicates when an external device can drive data on the bus.
*BS2, *BS3	Byte strobes	Output. Defines the byte lane of data on the data bus.
*TIP	Transfer in Progress	Output. Asserted to indicate a bus transfer is in progress. Negated during idle bus cycles.
*TA	Transfer Ack	Input with 4.7k pull-up to 3.3V. Indicates that the external data transfer is complete and should be asserted for one clock.
*TEA	Transfer Error Ack	Input with 4.7k pull-up to 3.3V. Indicates than an error condition exists for the bus transfer.

6.4 TIP Signal and External Data Bus Connections

The *TIP signal is the logical AND of *CS1, CS2 and *CS3. It can used to enable an external data bus buffer for the data bus signals. An example circuit design can be found on the MOD-DEV-100 Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 - D31



7 System Clock Signal

The Mod5270 uses a 14.7456 MHz crystal and onboard PLL to generate a system clock of 147.456 MHz. The address/data bus and clock output signal run at half the system clock speed, 73.728 MHz. If you are using the clock output signal we recommend you use a zero delay clock buffer (such as the ICS ICS574MLF) located as close to the Mod5270 clock output pin as possible.

8 UARTS

The Mod5270 has 3 UARTs, designated as UART 0, UART 1 and UART 2. All the UART signals go direct to the 5270 processor. It is recommended that you include a pull-up resistor of 10k ohms for any UART RX signals that are not used (either as UARTs or an alternate function).