### **Ethernet Core Module**

100 Version



# **DATASHEET**

### **Key Points**

 Use as a high-performance single board computer or add Ethernet connectivity to a new or existing design

### **Device Connectivity**

- 10/100Mbps Ethernet
- 2 UARTs and SPI
- SD/MMC flash card ready
- 29 digital I/Os

# Performance and memory

• 32-bit 62.5 MHz Processor

- Customize with a development kit and begin writing application code immediately!
- Industrial temperature range (-40°C to 85°C)
- 3 PWM
- 16-bit address bus and 16-bit data bus with 3 chip selects

• 8MB SDRAM and 2MB Flash

### Companion development kit

The following is available with the development kit:

- · Customize any aspect of operation including web pages, data filtering, or custom network applications
- Development software: NB Eclipse IDE, Graphical debugger, deployment tools, and examples
- Communication software: TCP/IP stack, SSL/TLS 1.3, HTTP web server, FTP, E-mail, and flash file system
- System software: NBRTOS, ANSI C/C++ compiler and linker





## **Specifications**

#### **Processor and Memory**

32-bit Freescale ColdFire 5272 running at 62.5MHz with 8MB SDRAM and 2MB Flash

#### **Network Interface**

10/100 BaseT with RJ-45 connector (100 Version)

### Data I/O Interface (J1 and J2)

- Up to 2 UARTs
- Up to 29 digital I/O
- Up to 2 external timer in and up to 3 timer outputs
- Up to 4 external IRQs

- 3 PWM
- SPI interface
- SD/MMC flash card ready
- 16-bit address bus and 16-bit data bus with 3 chip selects

### **Flash Card Support**

FAT32 support for SD Cards up to 8GB (requires exclusive use of SPI signals). Card types include SD/MMC (up to 2GB) and SDHC.

#### **Serial Configurations**

The UARTs can be configured in the following way:

- 2 TTL ports
- Add external level shifter for RS-232
- Add external level shifter for RS-422/485 (up to two ports)

Note: UART 0/1 also provides RTS/CTS hardware handshaking signals.

#### **LEDs**

Link and Speed (100 Version only, on RJ-45)

### **Physical Characteristics**

Dimensions (inches): 2.60" x 2.00" Mounting Holes: 2 x 0.125" dia

#### **Power**

DC Input Voltage: 3.3V @ 500mA typical

### **Environmental Operating Temperature**

-40° to 85° C

#### **RoHS Compliance**

The Restriction of Hazardous Substances guidelines ensure that electronics are manufactured with fewer environment harming materials.



### **Part Numbers**

MOD5272 Ethernet Core Module (100 Version, with RJ-45)

Part Number: MOD5272-100IR

#### **MOD5272 Development Kit**

Part Number: NNDK-MOD5272-KIT

Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents. Note: Includes the MOD-DEV-100 development board.

## **Ordering Information**

E-mail: sales@netburner.com Online Store: www.NetBurner.com Telephone: 1-800-695-6828



## **Pinout and Signal Description**

The module has two dual in-line 50 pin headers which enable you to connect to one of our standard NetBurner Carrier Boards, or a board you create on your own. Table 1-2 provides descriptions of pin function of the module header.

Table 1: Pinout and Signal Descriptions for J1 Connector (1)

	J1 Connector						
Pin	CPU Pin	Function 1	General Purpose I/O	Description	Max Voltage		
1		GND		Ground	-		
2		GND		Ground	-		
3		VCC3V		Input Power 3.3 VDC	3.3VDC		
4	P14	R/W		Read / NOT Write <sup>1</sup>	3.3VDC		
5	K10	CS1		Chip Select 11,2	3.3VDC		
6	P11	CS2		Chip Select 2 <sup>1,2</sup>	3.3VDC		
7	N11	CS3		Chip Select 3 <sup>1,2</sup>	3.3VDC		
8	P13	ŌĒ		Output Enable <sup>1</sup>	3.3VDC		
9	E12	BS2		Byte Strobe for D16 to D23 (8 bits) <sup>1</sup>	3.3VDC		
10	E13	BS3		Byte Strobe for D24 to D31 (8 bits) <sup>1</sup>	3.3VDC		
11		TIP		Transfer in Progress <sup>1,2</sup>	3.3VDC		
12	A5	D16		Data Bus - Data 16	3.3VDC		
13	F3	TA	PB5	Transfer Acknowledge <sup>1</sup>	3.3VDC		
14	A6	D18		Data Bus - Data 18	3.3VDC		
15	B6	D17		Data Bus - Data 17	3.3VDC		
16	В7	D20		Data Bus - Data 20	3.3VDC		
17	C7	D19		Data Bus - Data 19	3.3VDC		
18	A8	D22		Data Bus - Data 22	3.3VDC		
19	A7	D21		Data Bus - Data 21	3.3VDC		
20	F12	D24		Data Bus - Data 24	3.3VDC		
21	В8	D23		Data Bus - Data 23	3.3VDC		
22	F14	D26		Data Bus - Data 26	3.3VDC		
23	F13	D25		Data Bus - Data 25	3.3VDC		
24	G13	D28		Data Bus - Data 28	3.3VDC		
25	G12	D27		Data Bus - Data 27	3.3VDC		

- 1. Active low signals, such as RESET, are indicated with an overbar.
- 2. The TIP signal is the logical AND of  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$ . TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 D31.
- 3. J2-31 represents TIN0 and PB4/UART0 external baud rate clock. These two signals are tied together on the module PCB.
- 4. The ColdFire 5272 processor supports USB device mode only. A 48Mhz oscillator must be installed in locaton U8 of the Mod5272.



	J1 Connector (continued)						
Pin	CPU Pin	Function	General Purpose I/O	Description	Max Voltage		
26	H14	D30		Data Bus - Data 30	3.3VDC		
27	G14	D29		Data Bus - Data 29	3.3VDC		
28	M12	RESET		Processor Reset Input <sup>1</sup>	3.3VDC		
29	H13	D31		Data Bus - Data 31	3.3VDC		
30	F4	RSTOUT		Processor Reset Output <sup>1</sup>	3.3VDC		
31		CLK_OUT		Clock Out (CLKOUT-62.5 MHz)	3.3VDC		
32	D10	A0		Data Bus - Address 0	3.3VDC		
33	B12	A1		Data Bus - Address 1	3.3VDC		
34	A12	A2		Data Bus - Address 2	3.3VDC		
35	A13	A3		Data Bus - Address 3	3.3VDC		
36	A14	A4		Data Bus - Address 4	3.3VDC		
37	B13	A5		Data Bus - Address 5	3.3VDC		
38	B14	A6		Data Bus - Address 6	3.3VDC		
39	C12	A7		Data Bus - Address 7	3.3VDC		
40	C13	A8		Data Bus - Address 8	3.3VDC		
41	C14	A9		Data Bus - Address 9	3.3VDC		
42	D12	A10		Data Bus - Address 10	3.3VDC		
43	C11	A11		Data Bus - Address 11	3.3VDC		
44	B11	A12		Data Bus - Address 12	3.3VDC		
45	A11	A13		Data Bus - Address 13	3.3VDC		
46	C10	A14		Data Bus - Address 14	3.3VDC		
47	D9	A15		Data Bus - Address 15	3.3VDC		
48		VCC3V		Input Power 3.3 VDC	3.3VDC		
49		GND		Ground	-		
50		GND		Ground	-		

- 1. Active low signals, such as RESET, are indicated with an overbar.
- 2. The TIP signal is the logical AND of  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$ . TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 D31.
- 3. J2-31 represents TIN0 and PB4/UART0 external baud rate clock. These two signals are tied together on the module PCB.
- 4. The ColdFire 5272 processor supports USB device mode only. A 48Mhz oscillator must be installed in locaton U8 of the Mod5272.



Table 2: NetBurner MOD5272 Pinout and Signal Descriptions (4) for J2 Connector

	J2 Connector						
Pin	CPU Pin	Function 1	Function 2	General Purpose I/O	Description	Max Voltage	
1		GND			Ground	-	
2		VCC3V			Input power 3.3 VDC	3.3VDC	
3	H1	UART0_RX		PB1	UART 0 Receive	3.3VDC	
4	H4	UART0_TX		PB0	UART 0 Transmit	3.3VDC	
5		NC			No Connect	3.3VDC	
6	D11			PC14	Port C - Pin 14	3.3VDC	
7	E11			PC13	Port C - Pin 13	3.3VDC	
8	E10			PC15	Port C - Pin 15	3.3VDC	
9	G11			PC11	Port C - Pin 11	3.3VDC	
10	F11			PC12	Port C - Pin 12	3.3VDC	
11	H11			PC10	Port C - Pin 10	3.3VDC	
12	J13			PC9	Port C - Pin 9	3.3VDC	
13	J12			PC8	Port C - Pin 8	3.3VDC	
14		GND			Ground	-	
15	L2			PC0	Port C - Pin 0	3.3VDC	
16	L13			PC1	Port C - Pin 1	3.3VDC	
17	K12			PC4	Port C - Pin 4	3.3VDC	
18	L14			PC2	Port C - Pin 2	3.3VDC	
19	K13			PC5	Port C - Pin 5	3.3VDC	
20	K14			PC6	Port C - Pin 6	3.3VDC	
21	K1	UART1_RX	TOIN		UART 1 Receive or Timer Input 0	3.3VDC	
22	K4	UART1_TX	T0OUT		UART 1 Transmit or Timer Output 0	3.3VDC	
23	K11			PC3	Port C - Pin 3	3.3VDC	
24	J11			PC7	Port C - Pin 7	3.3VDC	
25	L5	SPI_CLK	BUSW1		SPI Clock or Bus Width Bit 1	3.3VDC	

- 1. Active low signals, such as RESET, are indicated with an overbar.
- 2. The TIP signal is the logical AND of CS1, CS2 and CS3. TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 D31.
- 3. J2-31 represents TIN0 and PB4/UART0 external baud rate clock. These two signals are tied together on the module PCB.
- 4. The ColdFire 5272 processor supports USB device mode only. A 48Mhz oscillator must be installed in locaton U8 of the Mod5272.



	J2 Connector (continued)							
Pin	CPU Pin	Function 1	Function 2	General Purpose I/O	Description	Max Voltage		
26	P1	SPI_CS3	T3OUT	PA7	SPI Chip Select 3 or Timer Output 3	3.3VDC		
27	P4	SPI_DIN			SPI Data In	3.3VDC		
28	N4	SPI_DOUT	WSEL		SPI Data Out or Bus Width Selection	3.3VDC		
29	H2	UARTO_CTS		PB2	UART 2 Clear To Send <sup>1</sup>	3.3VDC		
30	M5	SPI_CS0	BUSW0		SPI Chip Select 0 or Bus Width Bit 0	3.3VDC		
31	L6 , G3	TOIN	UART0_CLK	PB4	Timer Input 0 or UART 0 Clock <sup>3</sup>	3.3VDC		
32	N5	PWM0			PWM 0 Output Signal/Input Capture	3.3VDC		
33	E2	USB_TXEN		PA5	USB Transmit Enable	3.3VDC		
34	P5	PWM1	TOUT1		PWM 1 Output Signal/Input Capture or Timer Output 1	3.3VDC		
35	K2	SPI_CS2	UART1_CTS		SPI Chip Select 2 or UART 1 Clear To Send <sup>1</sup>	3.3VDC		
36	M6	TOOUT		PB7	Timer Output 0	3.3VDC		
37	K6	PWM2	T1IN		PWM 2 Output Signal/Input Capture or Timer Input 1	3.3VDC		
38	НЗ	UARTO_RTS		PB3	UART 0 Request To Send <sup>1</sup>	3.3VDC		
39	D2	USB_TP		PA0	USB Transmit Serial Data	3.3VDC		
40	L1	SPI_CS1		PA11	SPI Chip Select 1	3.3VDC		
41	F2	USB_D-			USB Line Driver Low	3.3VDC		
42	D1	USB_RP		PA1	USB Receive Serial Data	3.3VDC		
43	M4	ĪRQ1	USB_WOR		External Interrupt 1 <sup>1</sup>	3.3VDC		
44	F1	USB_D+			USB Line Driver High	3.3VDC		
45	N3	ĪRQ3			External Interrupt 3 <sup>1</sup>	3.3VDC		
46		GND			Ground	-		
47	КЗ	ĪRQ5	UART1_RTS		External Interrupt 5 <sup>1</sup> or UART 1 Request To Send <sup>1</sup>	3.3VDC		
48	МЗ	ĪRQ6		PA15	External Interrupt 6 <sup>1</sup>	3.3VDC		
49		GND			Ground	-		
50		VCC3V			Input Power 3.3 VDC	3.3VDC		

- 1. Active low signals, such as RESET, are indicated with an overbar.
- 2. The TIP signal is the logical AND of CS1, CS2 and CS3. TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 D31.
- 3. J2-31 represents TINO and PB4/UARTO external baud rate clock. These two signals are tied together on the module PCB.
- 4. The ColdFire 5272 processor supports USB device mode only. A 48Mhz oscillator must be installed in locaton U8 of the Mod5272.