MCF5213 Device Errata

Supports: MCF5211, MCF5212, MCF5213

This document identifies implementation differences between the MCF5213 microcontroller and the description contained in the *MCF5213 ColdFire® Microcontroller Reference Manual*. Refer to http://freescale.com/coldfire for the latest updates. The errata items listed in this document (summarized in Table 1) describe differences from the following documents:

- *MCF5213 ColdFire® Integrated Microcontroller Reference Manual*
- *ColdFire Microprocessor Family Programmer's Reference Manual*

The part number on the device can determine which errata have been corrected on a particular device as shown in Table 1.

All current MCF5211/12/13 devices are marked as M30B mask set.

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Table 1. Summary of MCF521x Errata

Errata ID	Module Affected	Date Errata Added	Device Affected	Errata Title
1	Clock	29 Apr 2005	PCF5213 PCF5212 PCF5211	Input Clock is Ignored When the External Oscillator is Configured as the Reference Clock
2	Clock	29 Apr 2005	PCF5213 PCF5212 PCF5211	Clock has Jitter of +/-10 Percent When PLL is Enabled
3	V_{STDBY}	27 Oct 2005	PCF5213 PCF5212 PCF5211 MCF5213 MCF5212 MCF5211	Non-functional RAM Standby Supply
4	Flash	17 Nov 2006	MCF5213 MCF5212 MCF5211	Internal Flash Speculation Address Qualification Incomplete
5	ADC	05 Feb 2008	MCF5213 MCF5212 MCF5211	ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively
6	ADC	05 Feb 2008	MCF5213 MCF5212 MCF5211	ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V
7	Debug	20 Mar 2008	MCF5213 MCF5212 MCF5211	Level 2 Trigger Operation Controlled by TDR[31]

1 Input Clock is Ignored When the External Oscillator is Configured as the Reference Clock

1.1 Description

When configuring the MCF5211/12/13 to use an external oscillator as the reference clock, the input clock is ignored and the clock output is generated from the on-chip oscillator (OCO).

1.2 Workaround

Place the MCF5211/12/13 into one of the external crystal modes (CLKMOD[1:0] = 01 or CLKMOD[1:0] = 11) and input an external oscillator on the EXTAL pin. If the PLL is enabled (CLKMOD[1:0] = 11), the valid external oscillator range is 2 to 10MHz. If the PLL is disabled (CLKMOD[1:0] = 01), the valid external oscillator range is 0 to 80MHz.

Part number affected: All devices with PCF prefix in the part number.

Workaround should not be applied to parts with MCF prefix in the part number.

2 Clock has Jitter of +/-10 Percent When PLL is Enabled

2.1 Description

When the PLL is enabled, the resulting clock has jitter of +/- 10 percent. This behavior is independent of the input clock source.

2.2 Workaround

Set bit 2 in the oscillator test register (IPSBAR + 0x120006) to 1 after powering on the processor. Take care not to disturb the other bit settings of this register. Therefore, bit 2 should be ORed into the default register setting.

Part number affected: All devices with PCF prefix in the part number.

Workaround should not be applied to parts with MCF prefix in the part number.

3 Non-functional RAM Standby Supply

3.1 Description

The V_{STDBY} supply is intended to supply power to the on-chip SRAM when the main power supply, V_{DD}, is removed. However, when V_{STDBY} is a higher voltage than V_{DD}, the V_{STDBY} supply sources power to the entire V_{DD} supply rail.

3.2 Workaround

V_{STDBY} should be connected to the V_{DD} supply. The STOP low-power mode should be used to conserve RAM contents and meet power savings requirements. V_{STDBY} should not exceed V_{DD} + 0.3V.

Part number affected: All devices.

4 Internal Flash Speculation Address Qualification Incomplete

4.1 Description

The flash controller uses a variety of advanced techniques, including two-way 32-bit bank interleaving and address speculation, to improve performance. An issue involving a complex series of interactions between the processor's local RAM (SRAM) and the local flash controller has been uncovered. In rare instances, the interaction between operand reads and writes to the SRAM and instruction fetches from the flash can result in incorrect data usage for a flash read operation. This may produce unexpected exceptions, incorrect execution, or silent data corruption.

The failing scenario includes the following:

1. A processor write to the local SRAM occurs at cycle *i*.

2. On the next cycle (cycle *i+1*), a processor read to the SRAM produces a 1-cycle read-after-write pipeline stall.
3. On the same cycle (cycle *i+1*), incorrect read data is selected for the flash access if both of the following situations occur:
   — There is a speculative flash access underway
   — The flash address and the SRAM read address have identical modulo-(flash_size) values

For example, on a device with a 256 Kbyte flash size, if flash_addr[17:0] equals sram_addr[17:0] and the other conditions are satisfied, incorrect read data is returned for the flash access.

4.2 Workarounds

4.2.1 Workaround One

Use FLASHBAR[6] to enable or disable the address speculation mechanisms of the flash controller. The default configuration (FLASHBAR[6] = 0) enables the address speculation. If FLASHBAR[6] equals 1, address speculation is disabled. Core performance may be degraded from 4% – 9%, depending heavily on application code.

NOTE

FLASHBAR[6] is user accessible via the movec instruction.
FLASHBAR[6] always reads back as 0.

4.2.2 Workaround Two

Construct the device memory map so the flash and SRAM spaces are disjoint within the modulo-(flash_size) addresses. This allows for flash speculation to remain enabled. If this approach is selected, it would typically require the upper portion of the flash memory be unused and the SRAM be mapped to this unused flash space.

Consider an example where the flash memory size is 256 Kbytes and the on-chip SRAM size is 32 Kbytes. If 224 Kbytes or less of flash are used, the SRAM can be based at the upper 32 Kbytes (within the modulo-256 Kbyte address) of the flash address space:

```
Flash: size = 0x40000, base = 0x0000_0000
RAM: size = 0x08000, base = 0x8003_8000 = RAM_BASE+(256-32) Kbytes
```

where the flash and SRAM base addresses are unique BA[31:16].

In summary, this approach can be applied if the combined size of the used flash and used SRAM is 256 Kbytes or less, with the flash contents justified to the lower address range and the SRAM contents justified to the upper address range.

4.2.3 Workaround Three

Separate the contents of the SRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR and RAMBAR to restrict accesses. This allows flash address speculation to remain enabled. For example, if the flash contains only instructions and the SRAM contains only

operands (all data), the appropriate address space mask fields are specified and speculation can remain enabled.

5 ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively

5.1 Description

The ADC could produce an error if the ADC reference voltage V_{REFH} is below the analog supply voltage V_{DDA}, or if the ADC reference voltage V_{REFL} is above analog ground V_{SSA} by more than 50 mV. The error is that the ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

5.2 Workaround

Connect V_{REFH} directly to V_{DDA}. Similarly, connect V_{REFL} to V_{SSA}.

6 ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V

6.1 Description

If the ADC reference voltage V_{REFH} is less than 3.1 V, either of the following error conditions could result:

- Low analog input voltages to the ADC might not be measured properly. (for example, input voltages less than 100 mV might yield measurements equal to 0)
- The ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

6.2 Workaround

Ensure that V_{REFH} is at or above 3.1 V.

7 Level 2 Trigger Operation Controlled by TDR[31]

7.1 Description

The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

7.2 Workaround

Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 — Level 2 trigger = PC_condition & Address_range & Data_condition
- 1 — Level 2 trigger = PC_condition | (Address_range & Data_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

Table 2. TDR[31:30] Definitions

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor Halt
10	PC_cond | (Add_range & Data_cond)	Debug Interrupt
11		Reserved

7.3 Status

Currently, there are no plans to fix this.

8 Document Revision History

Table 3 provides a revision history for this document.

Table 3. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
1.0	Added column toTable 1 showing part numbers affected. Also added statement that ‘MCF ‘prefix devices are not affected.
2.0	Added Section 3, “Non-functional RAM Standby Supply.” Updated Table 1.
2.1	Added “Part number affected: All devices” to Section 3, “Non-functional RAM Standby Supply.”
3	Added Section 4, “Internal Flash Speculation Address Qualification Incomplete.” Updated Table 1. Text changes for grammar and punctuation.
4	Added Section 5, “ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively” and Section 6, “ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V.” Updated Table 1.
5	Added errata: • Section 7, “Level 2 Trigger Operation Controlled by TDR[31]”

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Document Number: MCF5213DE
Rev. 5
03/2008

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