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Custom Baud Rates

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Introduction

The configuration web pages for the NetBurner standard/factory applications for serial communications typically have a maximum baud rate of 115,200, although much higher baud rates are possible. This is done because higher baud rates require a better understanding of system requirements. The UART baud rate on ColdFire processors can come from two different sources: a divisor of the system clock, or on some Modxxxx platforms, from an external oscillator fed into the appropriate signal pin. This application note will focus on the system clock divisor.

The OpenSerial() function call will take any integer value for a baud rate. However, since the divisor must be an integer value only certain baud rates are possible. This will vary by ColdFire processor type and system clock speed. Each processor type will be discussed. The intent of each section is to provide an overview and possible baud rates. Please reference the Freescale Users Manual for the processor you are using for additional details on UARTs and baud rate generation. A pdf version of these manuals are located in the c:\nburn\docs\FreescaleManuals directory of your development kit installation.

The associated Excel spreadsheet contains information on formulas and calculations for baud rates.

Software Design

Even though a very high baud rate can be configured in the baud rate registers, the maximum sustainable baud rate will be dependant on your application and overhead to do other tasks.

You may write your own serial drivers to enable custom baud rates, or modify the serial driver code located in \nburn\<platform>\system\serial.cpp in your NetBurner tools installation.

5272 Based Designs

The 5272 processor is used on the following platforms:

- SB72-300CR
- MOD5272-100IR
- SB72EX

System Clock: 62.5MHz, referenced as CLKIN
Number of UARTS: 2
FIFO Buffer: 24 bytes receive, 24 bytes transmit

The 5272 processor is unique because it has both a 16-bit system clock divider register (UDUn and UDLn), and a 4-bit fractional baud rate divider register (UFPDn) which provides a finer control over baud rates.

When CLKIN is the UART clocking source, it goes through a divide-by-32 prescaler and then passes through the 16-bit divider of the concatenated UDUn and UDLn registers, where 'n' references the specific UART.

Divider Equations:

UART Divider = CLKIN / (16 * 2 * BaudRate)
Fractional Divider = (truncated remainder * 16)

Example calculation for 230,000 baud:

UART Divider = 62.5MHz / (32 * 230000)
= 8.49
= 8 (truncate to lowest whole number)
UDUn = 0x00, UDLn = 0x08

Effective error = (.49/8) = 6.125%

Baud rate with only primary UART Divider = 62.5MHz / (16 * 2 * 8) = 244,140 baud

Fractional Divider = (.49 * 16)
= 7.84
= 8 (round to nearest whole number)
UFPDn = 0x08

Total %Error = 100 * (Truncated remainder) / (16 * (UD + UFPD/16)]
= 100 * (.84) / (16 * (8 + 8/16))
= 100 * .84 / 136
= 0.62%

5270 and 5234 Based Designs

The 5270 and 5234 processors are used on the following platforms:

- SB70LC-100IR
- SB70LC-200IR
- MOD5270-100IR
- MOD5270-200IR
- SB700EX-100CR
- MOD5234-100IR
- MOD5234-200IR
- CB34EX-100IR

System Clock: 147,456,000 Hz
System Bus Clock: 73,728,000 Hz
Number of UARTS: 3
FIFO Buffer: 4 bytes receive, 2 bytes transmit

The 5270 and 5234 processors have a 16-bit system clock divider register (UBG1n and UBG2n). When the system bus clock is the UART clocking source, it goes through a divide-by-32 prescaler and then passes through the 16-bit divider of the concatenated UBG1n and UBG2n registers, where 'n' references the specific UART. The minimum value for the 16-bit divider is 2.

Divider Equations:

UART Divider = SysBusClk / (32 * BaudRate)

Example calculation for 230,000 baud:

UART Divider = 73,728,000 / (32 * 230,000)
= 10.02
= 10 (truncate to lowest whole number)
UDUn = 0x00, UDLn = 0x0A

Actual baud rate = 73,728,000/ (32 * 10) = 230,400 baud

%Error = 0.17%

5282 Based Designs

The 5282 processor is used on the following platforms:

- MOD5282-100IR
- MOD5282-200IR

System Clock: 66,355,200 Hz
Number of UARTS: 3
FIFO: 4 bytes receive, 2 bytes transmit

The 5282 processor has a 16-bit system clock divider register (UBG1n and UBG2n). When the system clock is the UART clocking source, it goes through a divide-by-32 prescaler and then passes through the 16-bit divider of the concatenated UBG1n and UBG2n registers, where 'n' references the specific UART. The minimum value for the 16-bit divider is 2.

Divider Equations:

UART Divider = SysBusClk / (32 * BaudRate)

Example calculation for 230,000 baud:

UART Divider = 66,355,200 / (32 * 230000)
= 9.02
= 9 (truncate to lowest whole number)
UDUn = 0x00, UDLn = 0x0A

Actual baud rate = 66,355,200/ (32 * 9) = 230,400 baud

%Error = 0.17%